

Patent Abstracts of Japan

PUBLICATION NUMBER : 2002322592
PUBLICATION DATE : 08-11-02

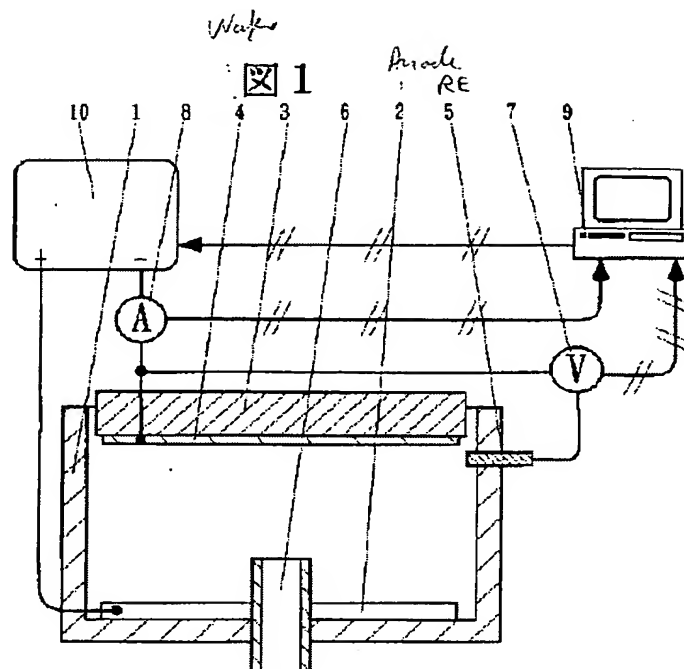
APPLICATION DATE : 24-04-01
APPLICATION NUMBER : 2001125361

APPLICANT : HITACHI LTD;

INVENTOR : MIYAZAKI HIROSHI;

INT.CL. : C25D 7/12 C25D 17/10 C25D 21/12
H01L 21/288 H01L 21/3205

TITLE : METHOD FOR MANUFACTURING
SEMICONDUCTOR DEVICE



ABSTRACT : PROBLEM TO BE SOLVED: To prevent film deposition defect due to plating by controlling the surface potential of a seed film.

SOLUTION: In a manufacturing method of a semiconductor device, in which a wafer is plated, the plating is performed by providing a reference electrode in the vicinity of the wafer and controlling applied voltage based on the surface potential of the wafer, which is obtained by the reference electrode. To be more specific, the surface potential is controlled to be negative to equilibrium potential in a 1st step, which is the initial time of the plating, and is controlled to be near the equilibrium potential in a 2nd step of the plating. As a result, the surface potential of the seed film is controlled highly precisely, the dissolution of the seed film is prevented and the strength of a high polymer coating film is made uniform and thus the film deposition defect of the plated film is prevented.

COPYRIGHT: (C)2003,JPO